



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/834,919 | 04/16/2001 | Hajime Akimoto | 503.40029X00 | 5427 |

20457 7590 11/10/2003

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER

NELSON, ALECIA DIANE

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2675

4

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

S.M. J.R.

Office Action Summary

Application No.

09/834,919

Applicant(s)

AKIMOTO ET AL.

Examiner

Alecia D. Nelson

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 April 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "5" and "10" have both been used to designate pixel. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The examiner request a clean copy of the specification submitted 11/27/01 including the marked changes as indicated in the submitted copy. The handwritten changes are too small and difficult to read.

A substitute specification filed under 37 CFR 1.125(a) must only contain subject matter from the original specification and any previously entered amendment under 37 CFR 1.121. If the substitute specification contains additional subject matter not of record, the substitute specification must be filed under 37 CFR 1.125(b) and must be

Art Unit: 2675

accompanied by: 1) a statement that the substitute specification contains no new matter.

Claim Objections

4. Claims 34 and 38 are objected to because of the following informalities: These dependent claims cannot be dependent from Claim X and Claim Y. The dependency should be Claim X or Claim Y. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. Claim 34 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim recites that the memory element is performed by; rewriting part of the display data output from the memory element to the data line, and then rewriting the display data from the data line. It is unclear as to how the rewriting the entire display after a portion has already been carried out.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2675

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. **Claims 1, 9, 11, 14-17, 21-23, 24, 26, 27, 29-31 and 36-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (U.S. Patent No. 5,627,557) in view of Tanaka et al. (U.S. Patent No. 5,594,464).

With reference to the **claim 1**, Yamaguchi et al. teaches a matrix of pixels (11a) is disposed in the liquid crystal panel (11), wherein each pixel (11a) is provided with a switching element. A scanning signal line driver (18) and data signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a group of signal lines and pixel switches (column 15, lines 67-19). A plurality of memory elements (sample hold circuit) for storing display data including a memory switch (1), a memory capacitor (CH) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63).

Art Unit: 2675

Yamaguchi et al. fails to specifically teach a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor. However, Yamaguchi does teach that timing is controlled to refresh each pixel so as to display an image based on a new data signal (see column 16, lines 46-55), wherein there is applied a refresh signal (see Fig. 16).

Tanaka et al. teaches a liquid crystal display device having a reset pulse applied in order to clear the previous display state before applying the signal for controlling the next display state (see column 19, lines 38-61).

Therefore it would have been obvious to one having ordinary skill in the art to allow the reset pulse as taught by Tanaka et al. in a device similar to that which is taught by Yamaguchi et al. which suggest usage of such reset pulse in order to remove any remaining charge or, in the case of gradation displays, remove any gradation from the pixel before applying the new gradation signal. This would thereby provide a display device that which the responding property of the liquid crystal is prevented from degrading.

With reference to **claim 9**, Yamaguchi et al. teaches that the memory capacitor (CH) is a capacitor between a gate and a channel of the amplifier (see Figures 1-2).

With reference to **claim 11**, Yamaguchi teaches that the other end of the memory capacitor is connected to a wire to which a preset voltage (5) is applied.

Art Unit: 2675

With reference to **claims 14**, Yamaguchi teaches that the other end of the memory capacitor is connected to a drain of the amplifier (see Figures 1-2).

With reference to **claim 15**, Yamaguchi teaches that the drain of the amplifier FET is connected to a voltage applying means (GND) (see Figures 1-2).

With reference to **claim 16**, Yamaguchi teaches that the source of the amplifier is connected to the voltage applying means (see Figure 1-2).

With reference to **claim 17**, Yamaguchi teaches that the plurality of basic units of the memory elements are connected to the data lines, and the amplifier FET is connected to the data line through a switch (1).

With reference to **claims 21-23**, Yamaguchi fails to specifically teach that the memory elements are arranged in a matrix along a group of data lines extending in a y-direction, wherein the memory switch and the selection switch in the individual units are connected to the same data line or data lines different from each other. Yamaguchi does teach that the pixels are arranged in a matrix and wherein elements (14, 15) have a single connection line that passes through each of the pixel elements. Moreover it is taught that the circuit structure of each pixel is not limited to the disclosed structure but includes the circuit structures according to other examples. (see Fig. 14, column 15, lines 10-19)

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the data line to connect both the memory switch and selection switch as taught by in by Yamaguchi or allow the memory switch and the selection switch to be connected to data lines different from each other as suggested by the teachings of Yamaguchi in order to provide a connection to the elements which allows the overall device to operated more efficiently.

With reference to **claim 24**, Yamaguchi et al. and Tanaka et al. fail to specifically teach a black matrix shielding means arranged between the transparent substrate corresponding to the back portions of the memory element and a lighting means. However, the usage of a black matrix is well known in the art.

With reference to **claims 26 and 27**, Yamaguchi et al. and Tanaka et al. fail to specifically teach that the image signal generating means comprises a D/A converter. However it is well known in the art for the data driver to include a D/A converter.

With reference to **claims 29-31 and 36-38**, Yamaguchi et al. teaches a matrix of pixels (11a) is disposed in the liquid crystal panel (11), wherein each pixel (11a) is provided with a switching element. A scanning signal line driver (18) and data signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a group of signal lines and pixel switches (column 15, lines 67-19). A plurality of memory elements (sample hold circuit) for

Art Unit: 2675

storing display data including a memory switch (1), a memory capacitor (C_H) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63). With further reference to **claims 32 and 35**, Yamaguchi et al. teaches amplifying a voltage level of the display data written in the data line and then rewriting the amplified voltage of the display data from the data line (see column 7, lines 25-34).

Yamaguchi et al. fails to specifically teach a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor. However, Yamaguchi does teach that timing is controlled to refresh each pixel so as to display an image based on a new data signal (see column 16, lines 46-55), wherein there is applied a refresh signal (see Fig. 16). Yamaguchi et al. fails to specifically teach refreshing by sequentially scanning, however this is a well known scanning technique.

Tanaka et al. teaches a liquid crystal display device having a reset pulse applied in order to clear the previous display state before applying the signal for controlling the next display state (see column 19, lines 38-61).

Therefore it would have been obvious to one having ordinary skill in the art to allow the reset pulse as taught by Tanaka et al. in a device similar to that which is taught by Yamaguchi et al. which suggest usage of such reset pulse in order to remove any remaining charge or, in the case of gradation displays, remove any gradation from the pixel before applying the new gradation signal. This would thereby provide a display

Art Unit: 2675

device that which the responding property of the liquid crystal is prevented from degrading.

9. **Claims 2-8, 10, 18-20, and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. and Tanaka et al. as applied to **claim 1** above, and further in view of Parks (U.S. Patent No. 5,471,225)

With reference to **claims 2**, Yamaguchi et al. teaches a driving circuit (20) which is disposed in the peripheral portion of the liquid crystal panel (11) (see column 16, line 2-5).

Yamaguchi et al. fails to specifically teach that the liquid crystal region is formed between the pixel electrodes and the counter electrode, however it is inherently known that the liquid crystal is located in such position to those skilled in the art.

Parks teaches the general construction of the LCD consisting of a pair of glass plates (22, 24), wherein the inside surface of glass panel (22) is a common electrode (30) and the inside of glass panel (24) is a pixel electrode wherein the liquid crystal (40) is located there between.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Tanaka et al., and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 3**, Yamaguchi et al. and Tanaka et al. also fail to teach that the plurality of display pixels have an optical reflecting plate, however this is well known in the art.

Parks teaches that the usage of alignment coatings and/or passivity coatings, are generally placed between electrode (30) and liquid crystal medium (40) as well as between each display electrode and liquid crystal medium.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Tanaka et al., and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 4**, Yamaguchi et al. teaches that the LC panel (11) occupies a display portion including a scanning signal and data signal line driver can be included in the display portion as shift registers (14, 15) and timing generating circuit (17) (see column 16, lines 12-17) thereby reducing the area need for the components, and in turn allowing the display area to be made smaller.

With reference to **claims 5 and 18-20**, Yamaguchi et al. teaches with reference to conventional art that the switching elements are TFTs (see column 1, lines 8-17).

With reference to **claims 6-8, 10, and 24**, Yamaguchi et al. and Tanaka et al. fail to teach that the switch or amplifier is of Poly-Si TFT type, however the usage of such type TFT is well known in the art. However, with further reference to **claim 10**, Yamaguchi teaches that the memory capacitor (CH) is a capacitor between a gate and a channel of the amplifier (see Figures 1-2).

Parks teaches that the gate of the TFT is deposited upon the substrate accordingly to the well-known methods (see column 6, lines 36-52).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Tanaka et al., and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

10. **Claim 28** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamuguchi et al, Yamazaki et al. (U.S. Patent No. 6,335,716) and Parks.

With reference to claim 28, Yamaguchi et al. teaches a matrix of pixels (11a) is disposed in the liquid crystal panel (11), wherein each pixel (11a) is provided with a switching element. A scanning signal line driver (18) and data signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a group of signal lines and pixel switches (column 15, lines 67-

Art Unit: 2675

19). A plurality of memory elements (sample hold circuit) for storing display data including a memory switch (1), a memory capacitor (CH) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63).

Yamaguchi et al. fails the specific usage of an image signal generating means, which has a reference voltage generating circuit using a poly-Si thin film resistor.

Yamazaki teaches a display device, which includes a control circuit, and transmits signals to, and from, the DSP and receives signals from the signal generator (see Figure 2)

Parks further teaches that the TFT is deposited upon the substrate according to the well-known methods (see column 6, lines 36-52).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the combination of Yamaguchi et al. Yamazaki, and Parks as described above in order to provide an improved arrangement for driving the display for the user to be able to view optimum display characteristics on the device.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday.

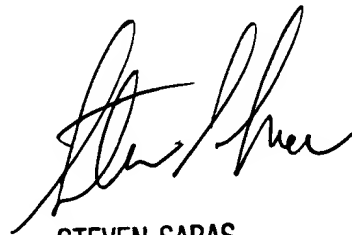
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720. The fax phone numbers for

Art Unit: 2675

the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

and/ADN
September 30, 2003

A handwritten signature in black ink, appearing to read 'Steven Saras', is positioned above the printed name and title.

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600